WHAT IS CLAIMED IS:

1. A programmable controller that performs sequential processing in accordance with execution codes generated by compiling a control program, said programmable controller comprising:

a storing unit which stores the execution codes; and

a universal microprocessor which mounts an acceleration mounting unit such as a pipeline logic and cache and which is directly executed by the execution codes.

2. A control-program-development supporting apparatus that develops a control program described with a sequential-control language such as a ladder diagram or instruction list, said control-program-development supporting apparatus comprising:

a compiler which compiles the control program into codes directly executable by a universal microprocessor that mounts acceleration mounting unit such as a pipeline logic and cache.

3. The control-program-development supporting apparatus according to claim 2 further comprising:

an optimization filtering unit which reconstructs the control program into an optimum code system by excluding not-cited variables and redundant codes and rearranging

codes for locally arranging instructions for a common input or output device is included,

wherein a control program optimized by said optimization filtering unit is newly used as the former control program.

4. The control-program-development supporting apparatus according to claim 2, further comprising:

a processing-time rough-estimating unit which has a relating table which relates a sample program having the processing time already known with the control program corresponding to the execution codes to estimate a sequential-processing execution time of a programmable controller in accordance with the relating table.

5. A control-program-development supporting apparatus that develops a control program described with a sequential-control language such as a ladder diagram or instruction list, said control-program-development supporting apparatus comprising:

a control-program dividing unit which divides the control program into a plurality of blocks; and

a compiler which compiles all or some of the blocks into execution codes directly executable by a programmable controller.

6. The control-program-development supporting apparatus according to claim 5,

wherein the programmable controller is provided with a universal microprocessor that mounts an acceleration mounting unit such as a pipeline logic and cache.

7. The control-program-development supporting apparatus according to claim 5,

wherein the control program is a ladder diagram or an instruction list generated from the ladder diagram, and

the control-program dividing unit divides the control program into a plurality of blocks at a predetermined rung in the ladder diagram to generate a program file every block concerned.

8. The control-program-development supporting apparatus according to claim 5,

wherein the control program is a ladder diagram or an instruction list generated from the ladder diagram, and

the control-program dividing unit divides the control program into a plurality of blocks at a predetermined rung serving as a jump destination for a jump instruction in the ladder diagram to generate a program file every blocks concerned.

9. The control-program-development supporting apparatus according to claim 5,

wherein the control program is a ladder diagram or an instruction list generated from the ladder diagram, and

the control-program dividing unit extracts all or some of rungs including instructions to a common input or output device from the ladder diagram, constitutes one block of all or some of the extracted rungs, and generates a program file every blocks concerned.

10. The control-program-development supporting apparatus according to claim 5 further comprising:

an optimization filtering unit which reconstructs the control program into an optimum code system by excluding not-cited variables and redundant codes and rearranging codes for locally arranging instructions for a common input or output device is included,

wherein a control program optimized by said optimization filtering unit is newly used as the former control program.

11. The control-program-development supporting apparatus according to claim 5, further comprising:

a processing-time rough-estimating unit which has a relating table which relates a sample program having the

processing time already known with the control program corresponding to the execution codes to estimate a sequential-processing execution time of a programmable controller in accordance with the relating table.

12. A control-program-development supporting apparatus that develops a control program described with a sequential-control language such as a ladder diagram or instruction list, said control-program-development supporting apparatus comprising:

a control-program dividing unit which divides the control program into a plurality of blocks;

a control-program converting unit which converts all or some of the blocks into advanced-language control programs described with a universal-computer-readable advanced language every blocks concerned; and

a compiler which compiles all or some of universal-computer-readable advanced programming languages corresponding every above block into directly executable codes by a programmable controller.

13. The control-program-development supporting apparatus according to claim 12,

wherein the programmable controller is provided with a universal microprocessor that mounts an acceleration

mounting unit such as a pipeline logic and cache.

14. The control-program-development supporting apparatus according to claim 12,

wherein the control program is a ladder diagram or an instruction list generated from the ladder diagram, and

the control-program dividing unit divides the control program into a plurality of blocks at a predetermined rung in the ladder diagram to generate a program file every block concerned.

15. The control-program-development supporting apparatus according to claim 12,

wherein the control program is a ladder diagram or an instruction list generated from the ladder diagram, and

the control-program dividing unit divides the control program into a plurality of blocks at a predetermined rung serving as a jump destination for a jump instruction in the ladder diagram to generate a program file every blocks concerned.

16. The control-program-development supporting apparatus according to claim 12,

wherein the control program is a ladder diagram or an instruction list generated from the ladder diagram, and